Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated circuit, comprising:

a bidirectional input/output circuit; and

an input circuit for receiving a signal, said input circuit having an activation input for receiving an activation signal to activate said input circuit, in a manner dependent on the activation signal, for receiving signals, said input circuit being contained in said bidirectional input/output circuit;

said input circuit being deactivated based on said activation signal such that the deactivated input circuit does not draw any quiescent or switching current as a result of the detection of received signals.

Claim 2 (original): The integrated circuit according to claim 1, wherein said input circuit may be switched on or off with an aid of the activation signal.

Claims 3 (cancelled).

Claim 4 (original): The integrated circuit according to claim 1,

wherein said input circuit has a data input for a memory circuit; and

further comprising a control circuit for generating the activation signal, said control circuit generating the activation signal when data are to be written to the memory circuit through said input circuit.

Claim 5 (currently amended): An integrated circuit, comprising:

an input circuit for receiving a signal, said input circuit having a data input for a memory circuit and an activation input for receiving an activation signal to activate said input circuit, in a manner dependent on the activation signal, for receiving signals, said input circuit being contained in a bidirectional input/output circuit;

said input circuit being deactivated based on said activation signal such that the deactivated input circuit does not draw

any quiescent or switching current as a result of the detection of received signals; and

a control circuit for generating the activation signal, said control circuit generating the activation signal when data are to be written to the memory circuit through said input circuit;

said control circuit generating the activation signal in a manner dependent on at least one of the following signals:

a circuit select signal;

a word line activation signal;

a bit line activation signal; and

a write signal.

Claim 6 (original): The integrated circuit according to claim 1, wherein the integrated circuit is an integrated memory circuit.

Claim 7 (previously presented): A method for activating an input circuit for an integrated circuit, which comprises the step of:

providing an integrated circuit according to claim 1;

activating the input circuit if a write access has been made to the integrated circuit; and

deactivating the input circuit if the write access has not been made to the integrated circuit.

Claim 8 (new): An integrated circuit, comprising:

an input circuit for receiving a signal, said input circuit having a data input for a memory circuit and an activation input for receiving an activation signal to activate said input circuit, in a manner dependent on the activation signal, for receiving signals; and

a control circuit for generating the activation signal, said control circuit generating the activation signal when data are to be written to the memory circuit through said input circuit;

said control circuit including:

at least a first logic device producing a first output related to the signal levels of a write signal and a bit line activation signal;

at least a second logic device producing a second output related to the signal levels of a memory select signal and a word line activation signal; and

at least a third logic device generating said activation signal based on said first output and said second output.

Claim 9 (new): The integrated circuit of claim 8, wherein said control circuit activates or deactivates said activation signal following a time delay after a change in signal level of at least one of the following signals:

a circuit select signal;

a word line activation signal;

a bit line activation signal; and

a write signal.

Claim 10 (new): The integrated circuit of claim 5, wherein said control circuit activates or deactivates said activation signal following a time delay after a change in signal level of at least one of the following signals:

a circuit select signal;

a word line activation signal;

a bit line activation signal; and

a write signal.

Claim 11 (new): An integrated circuit, comprising:

an input circuit for receiving a signal, said input circuit having a data input for a memory circuit and an activation input for receiving an activation signal to activate said input circuit, in a manner dependent on the activation signal, for receiving signals; and

a control circuit for generating the activation signal, said control circuit generating the activation signal when data are

to be written to the memory circuit through said input circuit;

said control circuit including:

a first inverter for receiving and inverting a write signal;

a second inverter for receiving and inverting a bit line activation signal;

a first NAND gate for receiving the inverted write signal and the inverted bit line activation signal, and producing a first output;

an inverter for receiving and inverting a memory select signal;

a second NAND gate for receiving the inverted write signal and for receiving a word line activation signal, said second NAND gate producing a second output; and

a NOR gate for receiving said first output and said second output and for generating an activation signal based on said first and second outputs.